Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A thin-film transistor comprising:

a substrate;

a semiconductor layer positioned on the substrate, the semiconductor layer comprising a channel region, two lightly doped drains, and two source/drain regions; and

a gate positioned on the substrate, the two lightly doped drains being symmetrically arranged with respect to the gate, either of the two gate edges being overlapped with the adjacent lightly doped drain, neither of the junctions between the lightly doped drains and the source/drain regions being overlapped with the gate, and neither of the source/drain regions being overlapped with the gate.

[c2] 2. The thin-film transistor of claim 1 wherein the gate is positioned above the semiconductor layer.

[c3] 3. The thin-film transistor of claim 1 wherein the gate is positioned below the semiconductor layer.

[c4] 4. The thin-film transistor of claim 1 further comprising an insulating layer positioned between the gate and the semiconductor layer.

[c5] 5. The thin-film transistor of claim 1 wherein the substrate comprises a glass substrate.

[c6] 6. The thin-film transistor of claim 1 wherein the gate comprises a length A, the channel region comprises a length B, the lightly doped drains comprise a length C, and a correlation among these lengths is as following: $B+0.2C \leq 0.5A \leq B+0.8C$.

[c7] 7. The thin-film transistor of claim 1 wherein the lightly doped drains have an equal length.

[c8] 8. The thin-film transistor of claim 1 wherein a length of the lightly doped drains is approximately between 0.3-3.5μm.

[c9] 9. A thin-film transistor comprising:
a substrate;
a semiconductor layer positioned on the substrate, the semiconductor layer comprising a channel region, two lightly doped drains, a source and a drain;
an insulating layer positioned on the semiconductor layer; and
a gate positioned on the insulating layer, the gate comprising a gate edge overlapped with the lightly doped drain adjacent to the drain, the gate being not overlapped with the junction between the lightly doped drain

and the drain, and the gate being not overlapped with the drain.

[c10] 10. The thin-film transistor of claim 9 wherein the gate comprises another gate edge overlapped with the lightly doped drain adjacent to the source, but the gate is not overlapped with the junction between the lightly doped drain and the source, and the gate is not overlapped with the source.

[c11] 11. The thin-film transistor of claim 9 wherein the substrate comprises a glass substrate.

[c12] 12. The thin-film transistor of claim 9 wherein the gate comprises a length A, the channel region comprises a length B, the lightly doped drain adjacent to the drain comprise a length C, and a correlation among these lengths is as following: $B+0.2C \leq 0.5A \leq B+0.8C$.

[c13] 13. The thin-film transistor of claim 9 wherein the lightly doped drains have an equal length.

[c14] 14. The thin-film transistor of claim 9 wherein a length of the lightly doped drains is approximately between 0.3-3.5μm.

[c15] 15. The thin-film transistor of claim 9 wherein the lightly doped drains are symmetrically arranged with respect to

the gate.